

REMARKS/ARGUMENTS

## 1. Rejection of claims 1-11 under 35 U.S.C. 102(b):

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Gupta et al (US 6,272,594).

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**Response:**

The applicant would like to point out the patentable differences between independent claims 1, 5, and 9 of the instant application and the Gupta reference. Each of the claims 1, 5, and 9 contains the limitation of "a single-channel memory controller" that is used to control data and control signals sent through first and second memory buses. By using a single-channel memory controller, the present invention allows motherboards originally designed for a two-channel memory controller to be controlled by a single-channel memory controller.

15 Gupta, on the other hand, does not teach the use of a single-channel memory controller, and instead teaches that the memory controller acts as a dual-channel memory controller. In column 6, lines 9-16, Gupta teaches that the memory controller provides separate memory buses that support independent simultaneous memory transactions. Therefore, Gupta does not teach the use of a single-channel 20 memory controller, as is recited in claims 1, 5, and 9.

25 For these reasons, claims 1, 5, and 9 are patentably distinguished from the prior art. Claims 2-4, 6-8, and 10-11 are dependent on claims 1, 5, and 9, and should be allowed if claims 1, 5, and 9 are allowed. Reconsideration of claims 1-11 is respectfully requested.

In view of the above arguments in favor of patentability, the applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

*Winston Hsu*

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Winston Hsu, Patent Agent No. 41,526

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : [winstonhsu@naipo.com](mailto:winstonhsu@naipo.com)

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